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Applicant:	Brintzinger, *et al.*	Docket No.:	2002 P 12234 US
Serial No.:	10/733,217	Art Unit:	2822
Filed:	December 11, 2003	Examiner:	Thomas, Toniae M.
For:	Method for Forming Three-Dimensional Structures on a Substrate		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Statement Regarding Translation Accuracy

Dear Sir:

A translation of the German Application, DE 102 58 094.4, filed December 11, 2002, is included herewith as Exhibit A and was used to prepare the instant application. The undersigned attorney has been informed and believes that Exhibit A is an accurate (literal) translation of the German priority application filed with the German Patent Office on December 11, 2002.

Respectfully submitted,

27 December 2006
Date

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Method for forming 3-D structures on wafers

The invention relates to a method for forming 3-D structures on wafers in the form of bumps distributed on the wafer, which are in each case electrically connected to a bonding pad on the wafer via an interconnect by realizing the 3-D structures and the interconnect by photolithographic processes by means of a photoresist mask patterned by exposure and development and by subsequent layer construction by metallization.

The increasing integration of semiconductor components and the continually rising number of electrical connections between wafers and the carrier elements thereof and, in particular, the required miniaturization in the sense of assemblies that are as flat as possible have led to the use of the direct contact-connection of the semiconductor chips on the carrier elements (e.g. flip-chip bonding).

However, in order to enable a direct contact-connection of semiconductor chips on carrier elements, such as a PCB (printed circuit board), it is necessary to produce on the semiconductor chip 3-D structures which end at their respective highest point in a gold-plated contact element and are connected to a bonding pad of the wafer via an interconnect. This gold-plated contact area may then be provided with a solder material and be electrically and mechanically connected to a corresponding soldering contact on the PCB.

In order to achieve a certain compensation of mechanical loading on the finished assembly, e.g. caused by different thermal expansion coefficients of the individual components, or during the handling thereof, the basic structure of the 3-D structure may be produced from a compliant material, e.g. silicone, thus resulting in a 3-dimensional, mechanically

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flexible structure which is fixedly connected to the wafer.

The interconnects (reroute layer) used for the electrical connection between the bonding pad and the 3-D structure are constructed on a seed layer, on which is grown a Cu interconnect and, above the latter, an Ni layer, which serves to protect the Cu layer from corrosion.

In order to achieve a solderability of the contact element, the Ni layer must be coated with gold in this region at least on the tip of the 3-D structure.

The required patterning of all the layers and functional elements is usually realized by photolithographic processes.

The functional elements are patterned after the deposition of a photoresist on the wafer e.g. by dispensing or printing and subsequent exposure and development of the said photoresist to produce a resist mask. A metallization made of Cu, Ni and Au may then be constructed within the openings of the resist mask on the seed layer. Afterwards, the gold layer must be partially covered by a lithography in such a way that the undesired regions of the gold layer can be selectively etched and, finally, all that remains is a gold layer on the tip of the 3-D structure.

This method can be represented in summary by the following process flow:

- deposition of the seed layer
- EPR1 (epoxy photoresist 1): coating and patterning of the EPR1 photoresist mask (lithography step 1)
- reroute plating, production of the Cu/Ni layer on the seed layer
- coating of the reroute layer with Au

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- EPR2 (epoxy photoresist 2): coating and patterning of the EPR2 photoresist mask (lithography step 2)
- selective etching of the Au layer (wet etching or removal/stripping)

In this method, the application of the photoresist is highly problematic owing to the 3-D structures on the wafer. The formation of the 3-D structures on the wafer leads to a greatly fissured surface, so that, during the application of a photoresist by the customary coating methods, such as printing or dispensing, it cannot be ensured that the thickness of the applied photoresist is the same at every point of the surface in spite of the structure of the wafer surface. Thus, it must be expected, for example, that the photoresist will run down at least partially on the 3-D structures and, consequently, have an excessively small thickness on the 3-D structures as a result. It must also be expected that the photoresist will uniformly fill, that is to say even out, depressions on the wafer, so that a larger thickness of the photoresist is to be noted in the region of the depressions.

However, in order to be able to produce structures suitable for subsequent processing steps, e.g. metallization, by means of the photolithography on the wafer, it must be ensured that the photoresist is distributed as uniformly as possible with the same thickness following the structure after the application on the wafer. That is particularly difficult in the case of 3-D structures, as already explained. The problems multiply if a plurality of photolithographic steps have to be carried out one after the other.

This problem also existed in a similar manner in the case of the photolithographic patterning of printed circuit boards (PCBs). The process of coating with a resist is effected by electrodeposition of an electrophoretic resist, in this case the entire printed

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circuit board being suspended perpendicularly into the electrophoretic resist. This is necessary in order to prevent the unavoidable outgasing of hydrogen from leading to disturbances of the coating (pinholes) during the coating operation. However, since it is absolutely necessary to prevent the rear side of the printed circuit board from likewise being coated with the resist, the rear side of the printed circuit board is covered with the aid of a film or the like prior to coating.

It has been shown, however, that transferring this method to the patterning of 3-D structures and a reroute layer on wafers in this way is not suitable since in practice it is virtually impossible to suspend the wafers perpendicularly into an electrophoretic resist and at the same time prevent the wafer rear side from being coated.

The invention is based on the object, then, of providing a method for forming 3-D structures on wafers which can be realized simply and reliably and with which a uniform coating with a completely uniform layer thickness is achieved over the surface of the wafer.

The formulated object on which the invention is based is achieved, in the case of a method of the type mentioned in the introduction, by virtue of the fact that an electrophoretic resist is used as the photoresist and the coating of the wafer with the electrophoretic resist is performed by dipping the active side of the wafer into the said resist, and by subsequently applying an electrical voltage between the wafer and the electrophoretic resist.

It has surprisingly been shown that it is possible to dip the wafer into the electrophoretic resist by the active side and to perform the desired coating with the photoresist by applying an electrical voltage. In

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particular, it has been shown that even very small structures on the wafer are coated with a uniform thickness.

Preferably, the active side of the wafer is dipped into the EPR in a horizontal arrangement of the wafer. This achieves a largely uniform distribution of the hydrogen bubbles over the area of the wafer.

Furthermore, the wafer rear side is protected from wetting during the process of dipping into the EPR, this being possible in a simple manner by means of suitable receptacle devices and exact positioning during the dipping operation.

In order to prevent gas bubbles from collecting on the surface of the resist during the layer deposition, the wafer may be caused to rotate during the coating operation into the EPR.

Another possibility consists in producing a flow in the electrophoretic resist at least below the wafer, so that the gas bubbles are transported away from the surface of the resist.

A favourable alternative consists in causing the electrophoretic resist to rotate in the region of the surface of the wafer, this rotation being able to be produced in a simple manner by means of a stirrer. This also enables the gas bubbles to be removed from the surface of the resist.

In a further refinement of the invention, the wafer is removed after the process of coating with the electrophoretic resist in a horizontal position and the coating is completed by a thermal treatment, for example baking or annealing. As a result, the coating acquires a sufficiently solid consistency whilst

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maintaining the uniform layer thickness, so that the wafer can be turned over and processed further.

The invention will be explained in more detail below using an exemplary embodiment. In the associated drawings:

Figure 1a shows a sectional illustration of a detail from a 3-D structure coated with a seed layer on a wafer;

Figure 1b shows the plan view of the 3-D structure according to Figure 1a;

Figure 2a shows a detail from the wafer coated with an electrophoretic resist;

Figure 2b shows the plan view of the wafer according to Figure 2a;

Figure 3a shows a detail from the wafer after the photolithographic patterning of the electrophoretic resist and the metallization of the interconnect;

Figure 3b shows the plan view of the wafer according to Figure 3a;

Figure 4a shows a detail from the wafer after the deposition of Au on the interconnect;

Figure 4b shows the plan view of the wafer according to Figure 4a;

Figure 5a shows a detail from the wafer after the stripping of the electrophoretic resist and the etching of the seed layer; and

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Figure 5b shows the plan view of the wafer according to Figure 5a.

Figures 1a, b illustrate a detail from a wafer 1, in which a compliant element 2 as basic element of the 3-D structure 3 to be produced is fixed on the wafer 1. In order to prepare for the subsequent metallization, a seed layer 4 is situated on the wafer and the compliant element 2. In order to be able to perform the metallization at the necessary locations on the wafer 1, an electrophoretic resist 5 is applied on the wafer 1. The coating of the wafer 1 may be performed by dipping the active side of the wafer into the electrophoretic resist situated in a container and by subsequently applying an electrical voltage between the wafer 1 and the electrophoretic resist in the container. Since, with increasing layer deposition on the wafer, the electrical resistance increases at the same time, the coating is automatically stopped after a sufficiently high resistance has been reached.

The active side of the wafer 1 is dipped into the electrophoretic resist in a horizontal position of the wafer 1. This results in a largely uniform distribution of the hydrogen bubbles over the area of the wafer 1 during the coating process. Furthermore, the rear side of the wafer must be protected from wetting during the coating operation, and this can be achieved in a simple manner by means of suitable receptacle devices and exact positioning during the dipping operation.

In order to prevent the gas bubbles from collecting on the surface of the resist 5 during the layer deposition, the wafer 1 may be caused to rotate during the coating operation. A comparable effect is achieved if a flow is produced in the electrophoretic resist at least below the wafer 1, so that the gas bubbles are transported away from the surface of the deposited resist 5. Thus, the electrophoretic resist could be

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FIG 1A

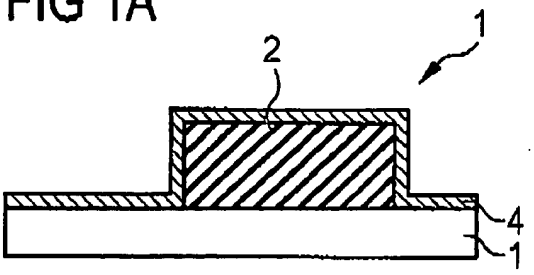

FIG 1B

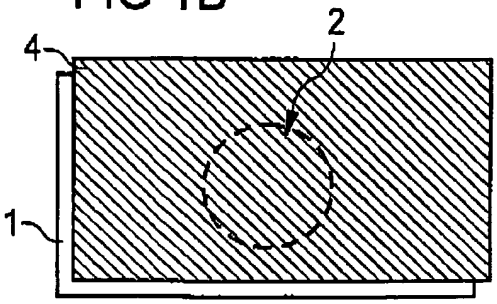

FIG 2A

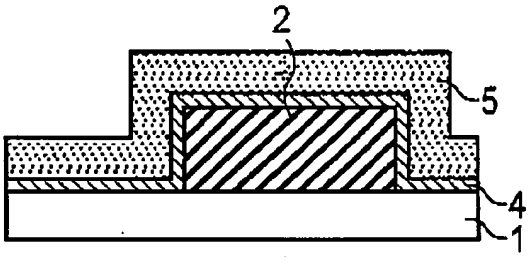

FIG 2B

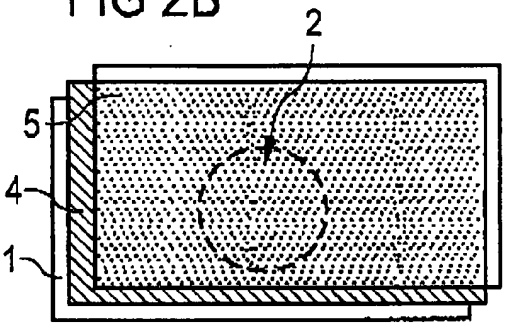

FIG 3A

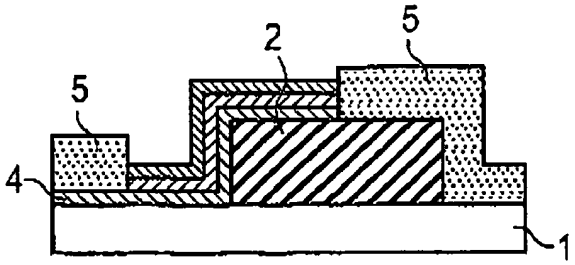

FIG 3B

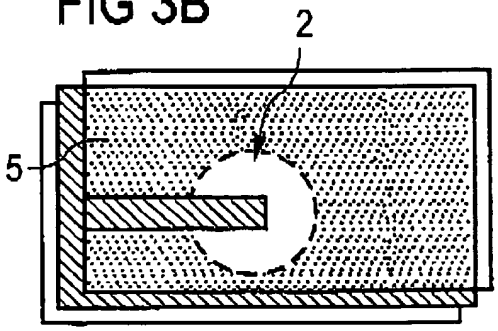

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FIG 4A

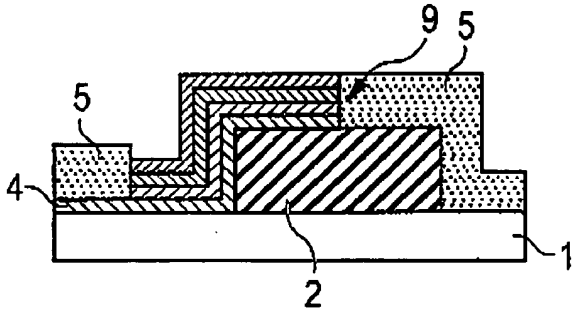

FIG 4B

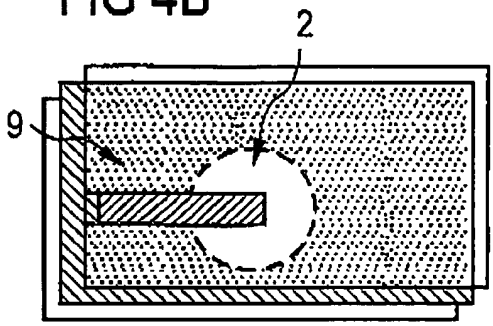

FIG 5A

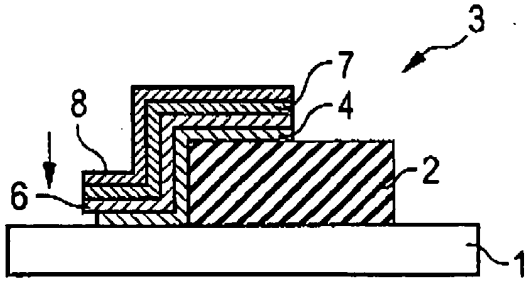

FIG 5B